87L Application on Long Transmission Line with Series Capacitor Banks and Shunt Reactors

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Abstract — Principles and applications of series capacitor banks and shunt reactors are first introduced. Then, the impacts of these apparatus on power systems are reviewed, including the behaviors of shunt reactors in the normal and fault conditions, the behaviors of series capacitor banks under the fault conditions. The effects of these apparatus on the line differential protection are particularly discussed. Challenges of relay applications are investigated with the emphasis on: advantages and disadvantages of including or excluding reactors in the 87L protection zone, solutions to compensate charging current, switching reactors in and out, voltage and current inversion of capacitor banks, sub-harmonic frequency transients, and effects of MOV conducting.

In order to demonstrate challenges of the relay application, a long transmission line is studied, where two series capacitor banks are installed at approximately one third intervals on the transmission line and two shunt reactor banks are installed at both ends. Two configuration schemes are presented. Arrangement of the line current differential communications channels to achieve maximum security and dependability is discussed. The settings selection of the line current differential relays is discussed in detail. A simple method to calculate charging current compensation settings for line differential protection is described as well.

Index Terms — Line Current Differential Relay, Shunt Reactor, Series Capacitor Bank

I. INTRODUCTION

A. *Application of shunt reactors*

A shunt reactor is a passive device connected at the ends of the long EHV transmission line or much shorter HV cable for the purpose of controlling the line voltage profile by compensating line shunt charging capacitance.

Considering a long EHV transmission line represented by the distributed parameter model as illustrated in Figure 1,

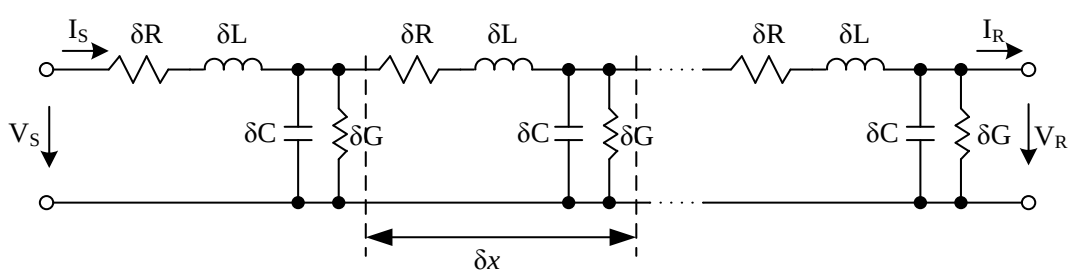

Figure 1. Distributed parameter transmission line model

where V_R and V_S are voltages at the receiving and sending terminals, I_R and I_S are currents at the receiving and sending terminals, x is the length of line section, R is the line series resistance, L is the line series inductance, G is the line shunt conductance, and C is the line shunt capacitance.

Whole line is equally divided into infinitesimally small sections, and the multiplier δ is the reciprocal of the amount of small sections.

Voltages and currents between the sending and receiving terminals are described as below [1],

$$\begin{bmatrix} V_R \\ I_R \end{bmatrix} = \begin{bmatrix} \cosh(\lambda x) & -Z_C \sinh(\lambda x) \\ -\dfrac{\sinh(\lambda x)}{Z_C} & \cosh(\lambda x) \end{bmatrix} \begin{bmatrix} V_S \\ I_S \end{bmatrix} \tag{1}$$

and,

$$\lambda = \sqrt{(r + jwl)(g + jwc)}$$

$$Z_c = \sqrt{\frac{r + jwl}{g + jwc}}$$

where λ is the propagation constant, Z_c is the surge impedance.

Taking the following transmission line as an example,

Voltage level: 500 kV

Length: 320 km

Positive sequence impedance: $Z_L = r + j\omega l = 116.37\ \Omega\angle 86.52^{o}$

Positive sequence capacitive reactance: $X_C = -j\omega c = -j1829.3\ \Omega$

Voltage profiles along the line at the different conditions are shown in Figure 2, where an ideal voltage source is presented at the sending terminal and the line is assumed as lossless.

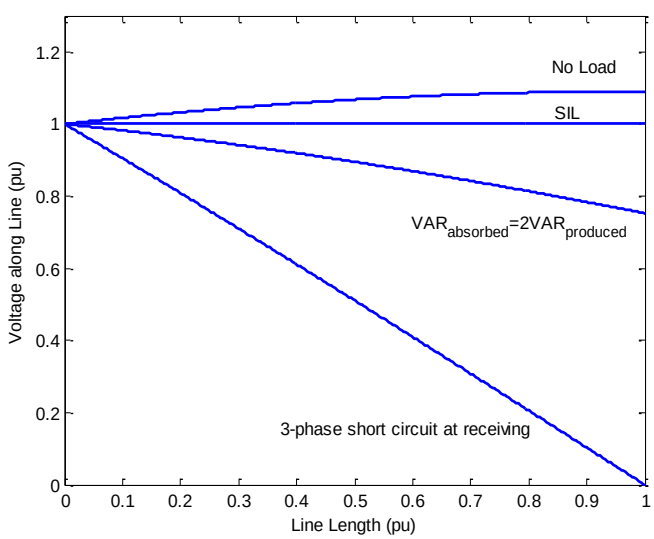

Figure 2. Voltage profile with no shunt reactor compensation

It is apparent that the voltage is increasing along the line at no load or light load condition. The reason is that the line shunt capacitance generates more reactive power than the line series inductance consumes, such that the excess of reactive power increases the voltage along the line. With the increase of the load current, the line inductance would absorb more reactive power, and when the current is greater than the Surge Impedance Loading (SIL) current, the shortage of reactive power would inversely decrease the voltage profile along the line. SIL of a transmission line is the power loading of a transmission line at which reactive power is neither produced nor absorbed, and is expressed as,

$$SIL = \frac{V_{L_L}^2}{Z_C} \tag{2}$$

The overvoltage in the light load condition may result in the following consequences:

- Increase of magnitude of transient voltage;
- Possible nuisance of overvoltage relays;
- Overstressing of insulation of power equipment;
- Overexcitation of power transformers.

In order to avoid overvoltage during the light load condition, the shunt reactor is normally connected in parallel with the line shunt capacitance to absorb the excess reactive power. Assuming a reactor is connected at the point x_1, the voltages and currents between the sending and receiving terminals are then described as below,

$$\begin{bmatrix} V_R \\ I_R \end{bmatrix} = \begin{bmatrix} \cosh(\lambda x_1) & -Z_C \sinh(\lambda x_1) \\ -\dfrac{\sinh(\lambda x_1)}{Z_C} & \cosh(\lambda x_1) \end{bmatrix} \begin{bmatrix} 1 & 0 \\ -\dfrac{1}{jX_{Reactor}} & 1 \end{bmatrix} \bullet \begin{bmatrix} \cosh(\lambda x_2) & -Z_C \sinh(\lambda x_2) \\ -\dfrac{\sinh(\lambda x_2)}{Z_C} & \cosh(\lambda x_2) \end{bmatrix} \begin{bmatrix} V_S \\ I_S \end{bmatrix} \tag{3}$$

$$x_1 + x_2 = x$$

where, $X_{Reactor}$ is the reactance of the shunt reactor and x is the length of the line.

Assuming two identical shunt reactors are installed at both terminals of the same line above, which can provide 70% compensation in total, and the reactance of one reactor is *j1965.2* Ω. Similarly, the voltage profiles along the line at the no load condition are shown in Figure 3.

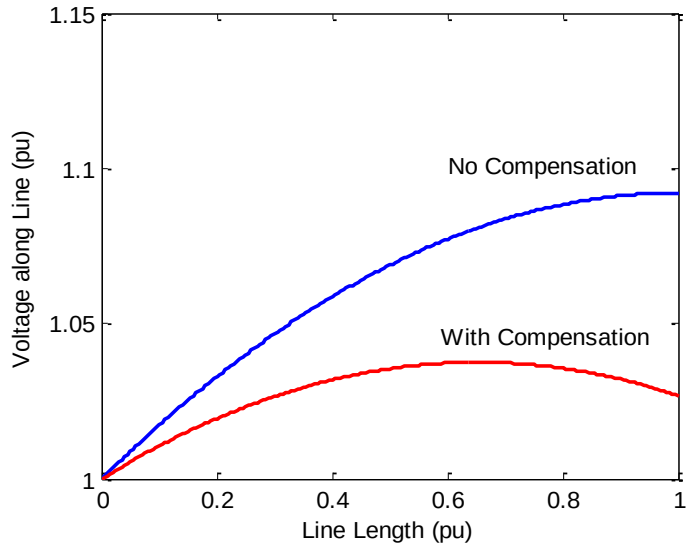

Figure 3. Voltage profile when shunt reactor compensation applied

It can be observed that the receiving voltage is reduced to 102.7% of the sending voltage from 109.2% without shunt reactors.

If changing the compensation degree of reactor from 0% to 100%, the receiving voltage and the maximum voltage along the line are illustrated in Figure 4. It can be observed that the maximum voltage along the line is not always occurring at the receiving end.

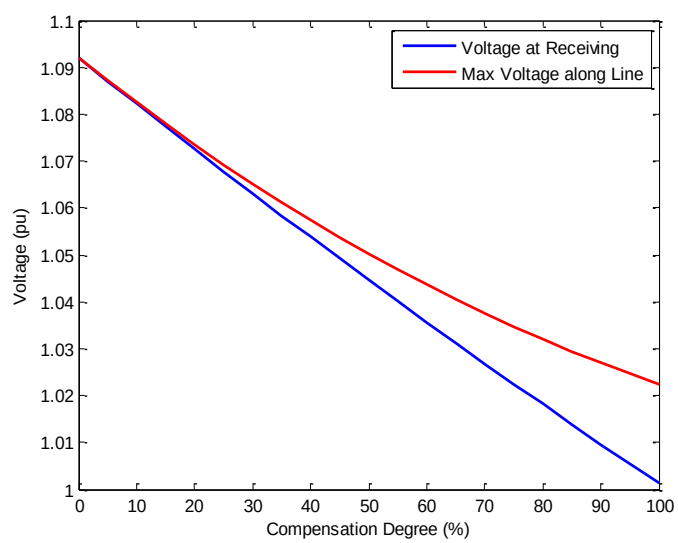

Figure 4. Receiving voltage and maximum voltage along line using different compensation degrees

It should be mentioned that the receiving voltage is around 100.1% of the sending voltage in Figure 4 rather than exact 100%, under the 100% compensation. This is caused by the modeling difference between the lumped inductance compensation and distributed line capacitance.

The benefits of application of shunt reactors are summarized as below.

- Reduce voltage increase, limit the operating voltage within the desired margin, and contribute to the voltage stability of the system;
- Reduce overvoltage on healthy phases following a single line-to-ground fault;
- Absorb reactive power, thus increase the energy efficiency of the system;
- Prevent overvoltage caused by generator self-excitation on capacitive loads;
- Prevent overexcitation of power transformers caused by overvoltage;
- Suppress secondary arc with the installation of a neutral reactor, then allow for successful reclosing for transient line faults.

B. ***Application of series capacitor banks***

Series capacitor bank is connected at the ends of or along the long EHV transmission line for the purpose of increasing power transfer capacity by compensating the line series inductance [2].

The power transfer across a line can be described as,

$$P = \frac{V_1 * V_2}{X_L} sin(\delta) \tag{4}$$

where, V_1 and V_2 are voltages at both ends, X_L is line series reactance, and δ is the voltage angle difference.

With the installation of a capacitor bank, the power transfer is given as,

$$P = \frac{V_1 * V_2}{X_L - X_C} sin(\delta) \tag{5}$$

Therefore, it can be concluded that:

- under the same voltage conditions, the power transfer capacity can be increased, additionally,
- under the same requirement of power transfer capacity, the angular stability can be increased.

The series capacitor bank can improve the voltage profile of the line as well. The line reactance consumes more reactive power when load current increases, which would result in the lower voltage along the line. However, if the series capacitor bank is installed, it can provide more reactive power, which can improve the voltage profile, especially in the heavy load condition. This process is dynamically adjusted, depending on the load current.

Similarly, assuming a capacitor bank is connected at the point x_1, the voltages and currents between sending and receiving terminals are then described as below,

$$\begin{bmatrix} V_R \\ I_R \end{bmatrix} = \begin{bmatrix} \cosh(\lambda x_1) & -Z_C \sinh(\lambda x_1) \\ -\dfrac{\sinh(\lambda x_1)}{Z_C} & \cosh(\lambda x_1) \end{bmatrix} \begin{bmatrix} 1 & -\dfrac{1}{jX_{Capacitor}} \\ 0 & 1 \end{bmatrix}$$
$$\bullet \begin{bmatrix} \cosh(\lambda x_2) & -Z_C \sinh(\lambda x_2) \\ -\dfrac{\sinh(\lambda x_2)}{Z_C} & \cosh(\lambda x_2) \end{bmatrix} \begin{bmatrix} V_S \\ I_S \end{bmatrix} \tag{6}$$
$$x_1 + x_2 = x$$

where, $X_{Capacitor}$ is the reactance of the series capacitor.

Assuming two identical series capacitor banks are installed at the one-third and two-third of the line, which can provide 60% compensation in total. The reactance of one capacitor is *-j34.96* Ω.

A simple example is given below to show the voltage profile along the line at the heavy load condition with and without series compensation.

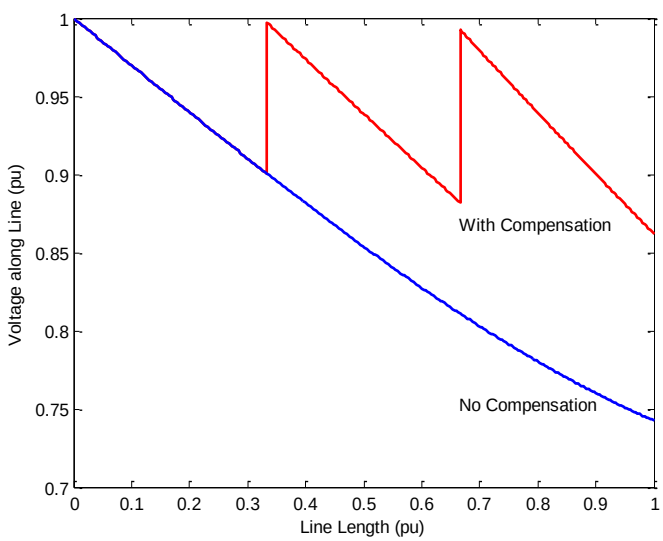

Figure 5. Voltage profile when series capacitor compensation applied

Normally, in the EHV application, the series capacitor bank consists of a set of capacitor units and the protective components [3], as shown in Figure 6.

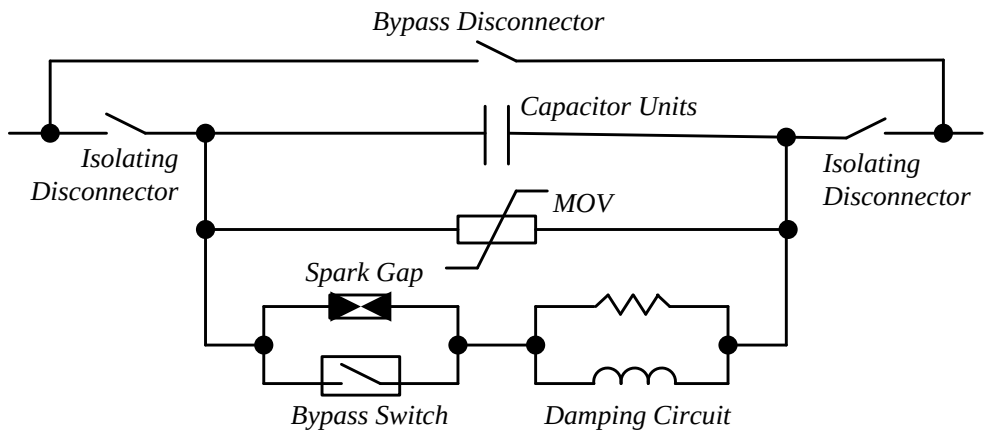

Figure 6. Diagram of series capacitor bank

The capacitor units include a set of small size capacitors in series and in parallel. The units are equipped with internal fuses. The Metal Oxide Varistor (MOV) is applied to reduce overvoltage across the capacitor without entirely bypassing the capacitor during a fault occurring outside of the capacitor circuit, such that the capacitor can continue to be in service during fault and the stability of the transmission system is maintained. Once the voltage exceeds a certain value or the absorbed energy by MOV exceeds its rated thermal threshold, the spark gap is forced triggered to bypass the capacitor. The damping circuit consists of a reactor with a parallel-connected resistor. They are used to control the capacitor discharge current and reduce the voltage across the capacitor after a bypass operation. The reactor is to limit the current since it behaves like large impedance during abrupt current transients. The resistor is to add damping to the capacitor discharge current. After capacitor bank is bypassed, it will be brought back into service once capacitors are discharged and MOV is cooled down.

II. EFFECTS ON POWER SYSTEMS

A. *Effects of shunt reactors*

The benefits of application of shunt reactors has been discussed in Section I-A. The characteristics and behaviors of shunt reactors introduce the impacts on power systems in the normal operating conditions and faulty conditions. The same system used in Section I-A is studied in this section.

1) *Normal operating conditions*

a) *Overvoltage and core saturation*

Unlike transformer where the knee point is normally designed around 1.1 pu, usually, the knee point of a reactor is around 1.25-1.35 pu and the slope of the saturated part is 20% to 40% of the slope in the unsaturated region [4]. Therefore, it is unlikely that the magnetic-core reactor would experience core saturation under the same overvoltage condition. Even this type of reactor does saturate, the induced harmonics have very small effects and no practical impairment on the performance of protections.

The following example compares the magnetizing currents of transformer and reactor during core saturation caused by overvoltage. It can be observed that the third and fifth harmonics are dominant in the reactor saturation. In the neutral point of the reactor, the third harmonics would act like a zero sequence current.

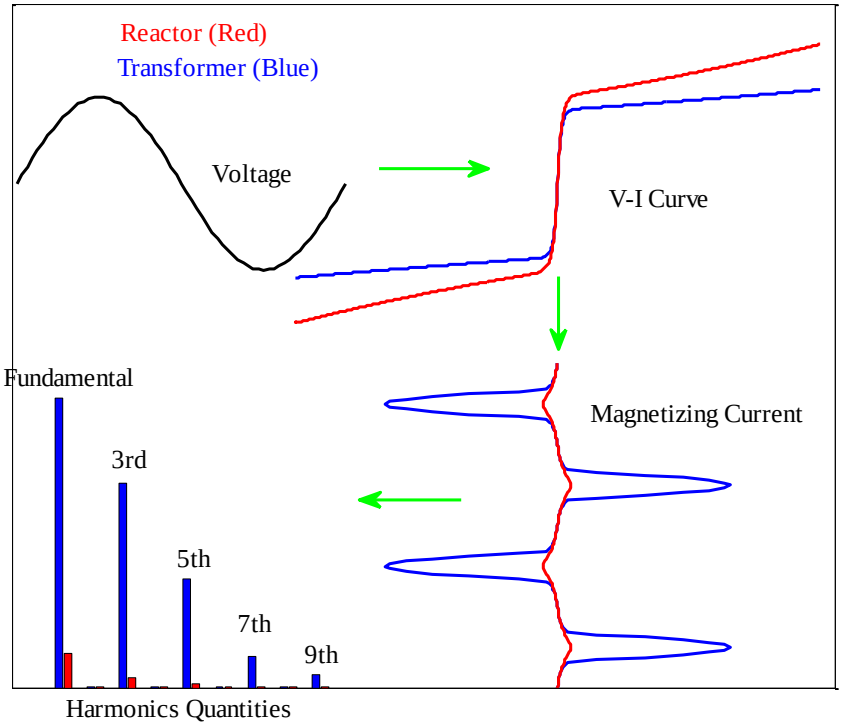

Figure 7. Magnetizing currents of transformer and reactor during overvoltage

b) ***Switching-in***

Similarly to the other devices with the magnetic material, the magnetic-core reactors are prone to inrush currents during the process of switching-in. However, due to the larger linear operating region and less dynamically changed slope, usually, reactors generate the slightly distorted current but with a significant dc component, unlike the inrush current in a transformer which contains a large amount of the second and fourth harmonics.

The following figure illustrates the phase currents of shunt rector during a 3-pole simultaneous switching-in, where the phase-A is closed at the instant of voltage zero-crossing and all three phases are closed at the same time. It can be observed that the reactor does experience the core saturation. The peak current of phase-A increases up to 5.16 times rated current, rather than 2.828 times under the unsaturation condition. The waveforms are slightly distorted by the harmonics, but much heavily by the dc offset. All three phases experience different degrees of dc offset, which is most influenced by the angle of the voltage when the reactor is energized. Additionally, the particular reactor parameter will also affect the peak current value. The dc offset takes several seconds to decay because of the quite large time constant (higher X/R ratio) of reactors.

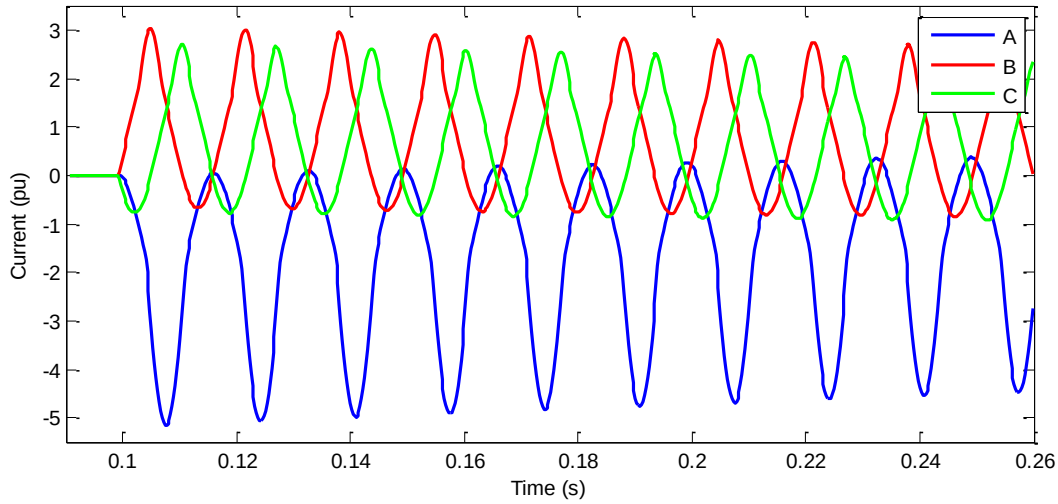

Figure 8. Phase currents of reactor during a 3-pole simultaneous switching-in

The neutral current and its fundamental magnitude are shown below as well. Since the inrush currents in the three phases are unbalanced, there exists the zero sequence current in the neutral, which may cause misoperation of the neutral current protection.

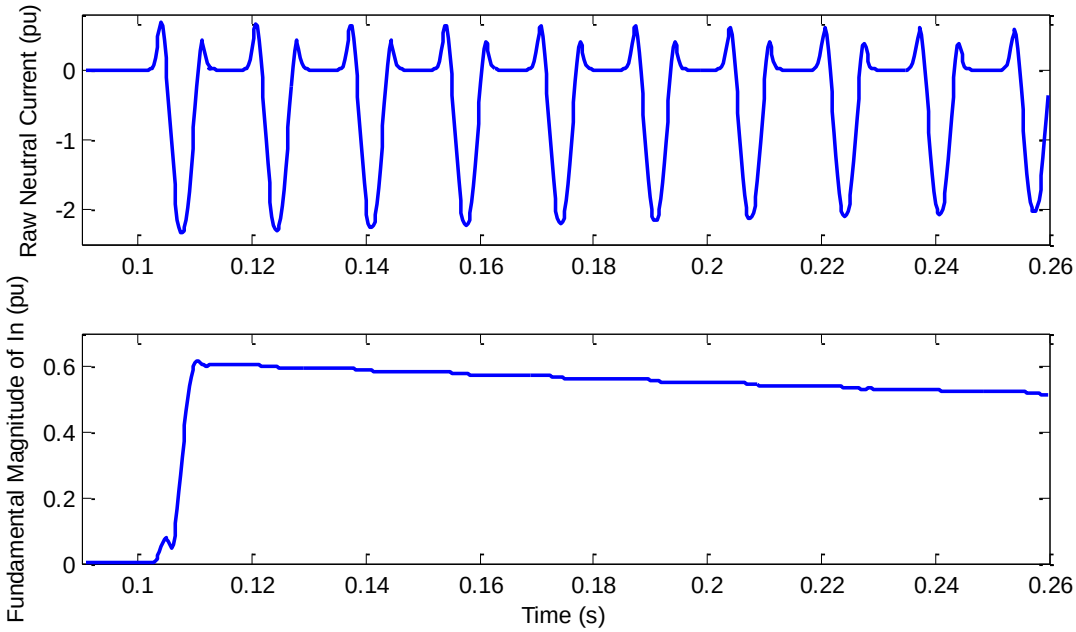

Figure 9. Neutral current of reactor during a 3-pole simultaneous switching-in

However, the synchronized switching-in strategy can be adopted, where three circuit breaker poles must be precisely closed at three consecutive phase voltage peaks. The phase and neutral currents are illustrated below.

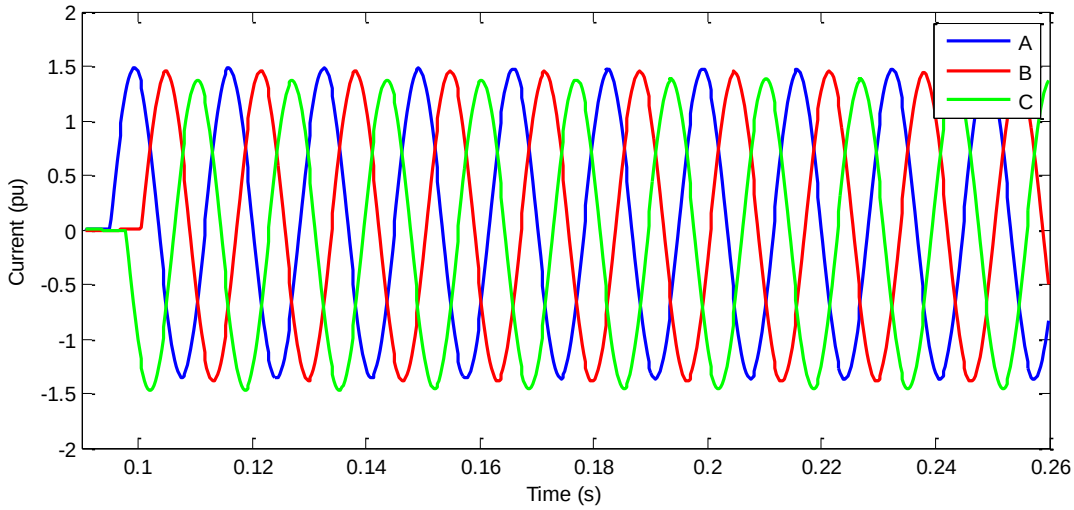

Figure 10. Phase currents of reactor during a synchronized switching-in

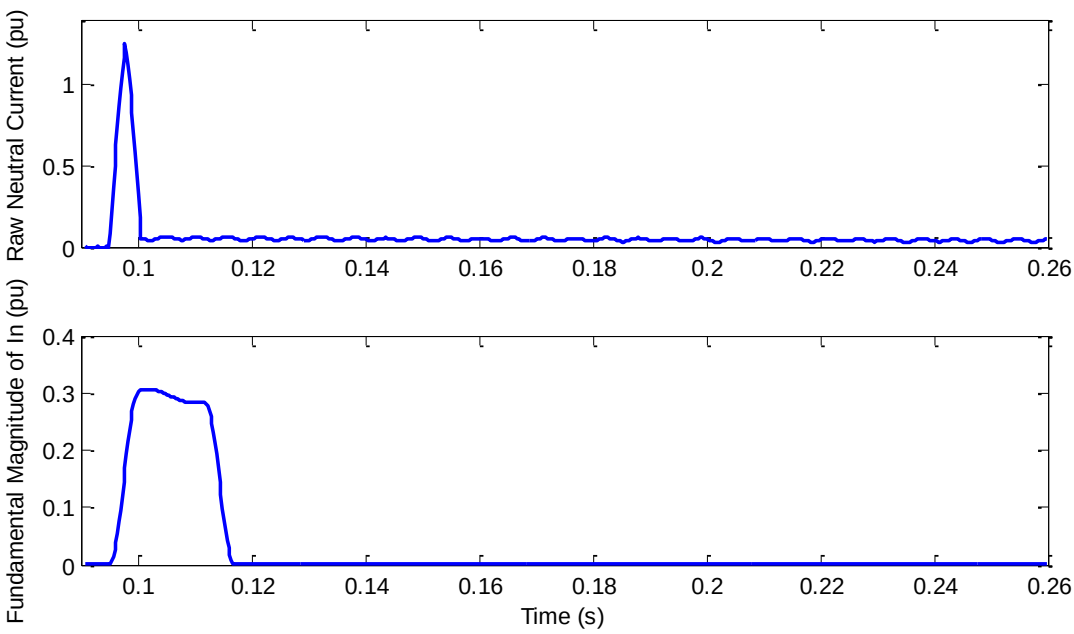

Figure 11. Neutral current of reactor during a synchronized switching-in

2) *Fault conditions*

The scenarios analyzed in this section assume that:

- the reactor is connected on the line, and
- the reactor circuit breaker does not isolate the reactor from the line during faults. The faults discussed in this section are referred to the faults occurring outside of the reactor, rather than the internal faults within the reactor.

a) *Resonance with line capacitance*

After clearing a fault by a three-pole tripping of the line circuit breaker, the healthy phase(s) of the shunt reactor will start resonance with the line shunt capacitance. The following figure shows an example, where voltages of phase-B and phase-C experience resonance after tripping all three phases caused by a phase-A to ground fault.

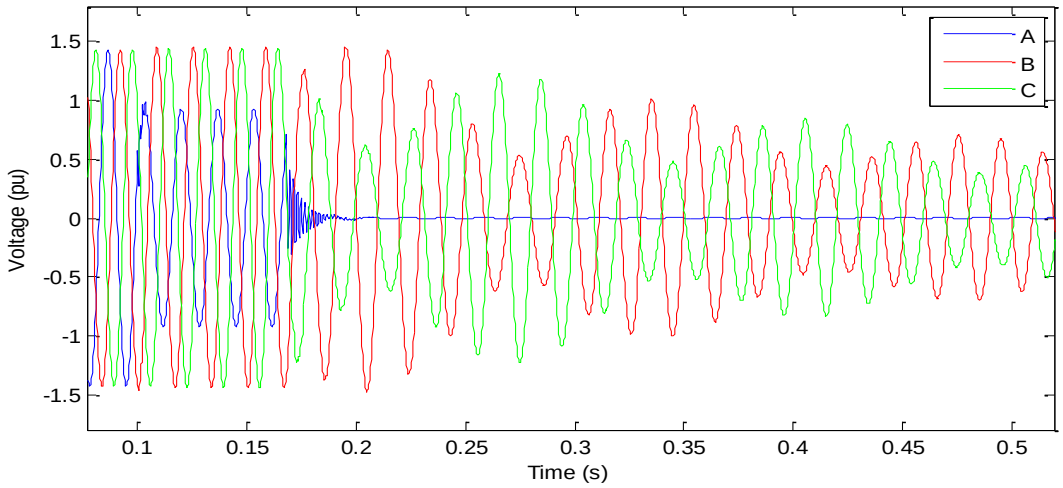

Figure 12. Voltage resonance in healthy phases after tripping all three phases

It is well known that the resonance frequency for a simple LC circuit in parallel can be calculated by the following equation,

$$f_R = \frac{1}{2\pi\sqrt{LC}} \tag{7}$$

Assuming an ideal situation, the above equation can be approximated to

$$f_R = f_0\sqrt{\frac{\eta}{100}} \tag{8}$$

where, η is the compensation degree in percentage, and f_0 is the nominal frequency.

For example, if the compensation degree is 70%, the resonance frequency would be 50.2 Hz. The following figure shows the raw frequency of resonated phases, which is calculated by the simple zero-crossing method. Due to the factor of distributed line capacitance and reactance in the real transmission line, it is expected that the average of the true frequency may be slightly different from the ideal one in Eq. (8).

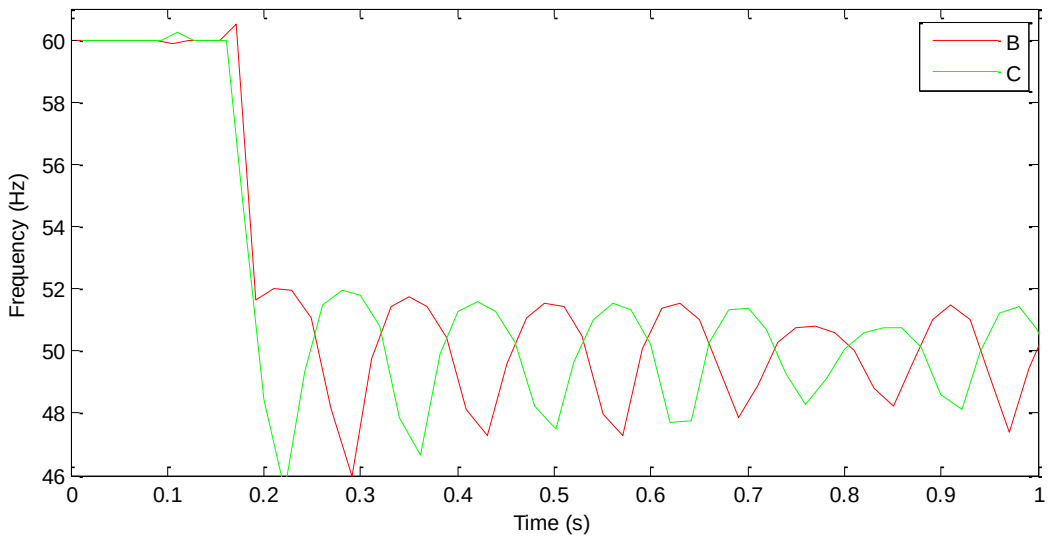

Figure 13. Estimated resonance frequency

b) ***Transients during faults and after clearing faults***

During a fault condition, since the voltage of the faulty phase decreases, the reactor phase current is reduced as well and the dc component may be induced into the fault current depending on the fault inception angle, as shown in Figure 14. After clearing the fault, the currents in the healthy phases would start oscillating developing consistent pattern for frequency of voltages as shown in Figure 12.

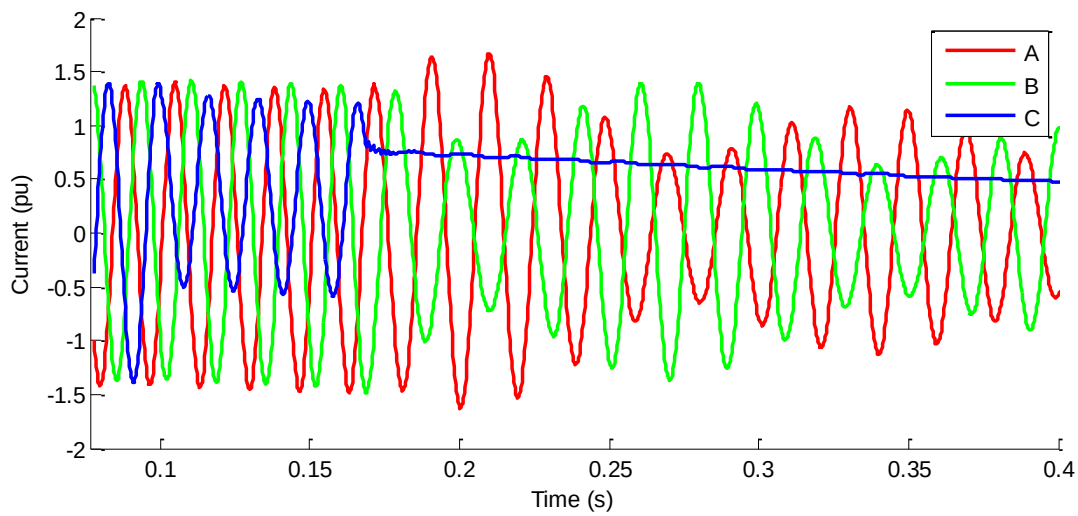

Figure 14. Phase currents of reactor during a fault and after clearing fault

As a result, the neutral current would reflect the unbalance among three phases, as shown in Figure 15.

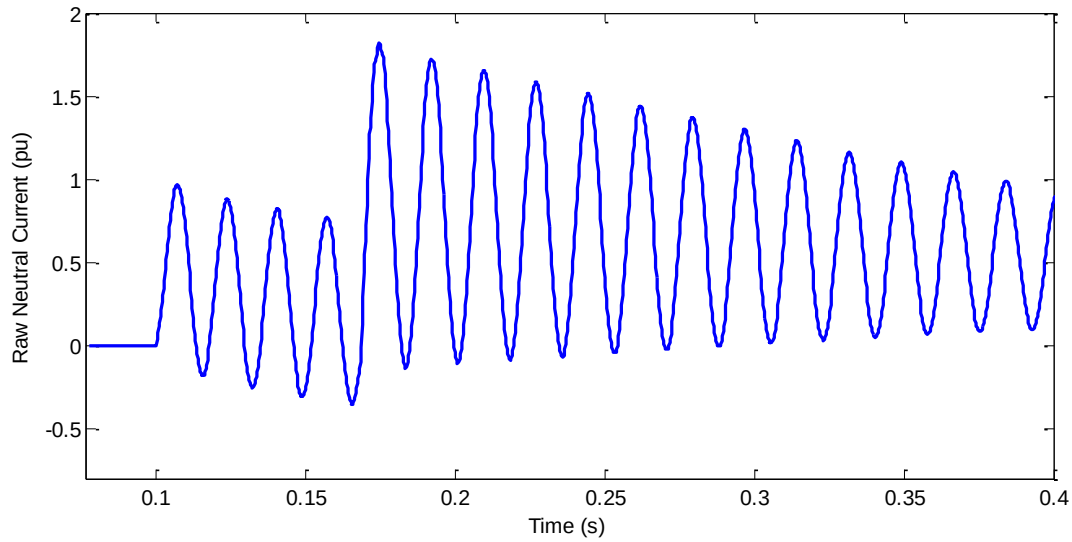

Figure 15. Neutral current of reactor during a fault and after clearing fault

c) ***Zero sequence infeed***

The apparatus with the grounded neutral can be source of the zero-sequence current during ground faults or system unbalance. The shunt reactor is one of these apparatus. Naturally, the zero-sequence source impedance, zero-sequence reactor reactance and lumped zero-sequence line capacitance are connected in parallel in the zero-sequence network, having the same zero sequence voltage drop. Therefore, the larger impedance element would absorb the smaller portion of the total zero sequence current. Due to the quite larger value of the zero-sequence reactor reactance, the reactor would absorb negligible amount of the zero-sequence current. The ratio between the zero sequence current flowing into the LC parallel circuit and the zero sequence current flowing into the source can be approximated by the following equation,

$$\begin{aligned}\frac{I_{0_LC}}{I_{0_SRC}} &= Z_{0_SRC}Y_{0_LC} \\ &= Z_{0_SRC}(-j)(Y_{0_L}-Y_{0_C})\end{aligned} \tag{9}$$

If there is no neutral reactor connected (neutral point is directly grounded), $Y_{0_L}=1/X_{1_L}$, otherwise, $Y_{0_L}=1/(X_{1_L}+3X_N)$. Three factors can be found from the above equation,

- The ratio is basically depending on the zero sequence source impedance since the line susceptance and reactor reactance are almost constant. The weaker system would result in the larger ratio.
- If the neutral reactor is connected, the ratio will become smaller.
- Basically, this ratio is quite small. In the simulation, this value is around 1.45% with a neutral reactor and 2.29% with no neutral reactor.

B. *Effects of series capacitor banks*

The application of series capacitor banks has been discussed in Section I-B. This section presents the impacts of series capacitor banks on power systems. The full cycle DFT technique is used to calculate the phasor in this paper. In the real implementation of relays, some filtering techniques may be applied to remove dc decaying or other transients.

1) *Voltage inversion*

Considering the following system with the series capacitor bank located at the left line side of the bus *R*.

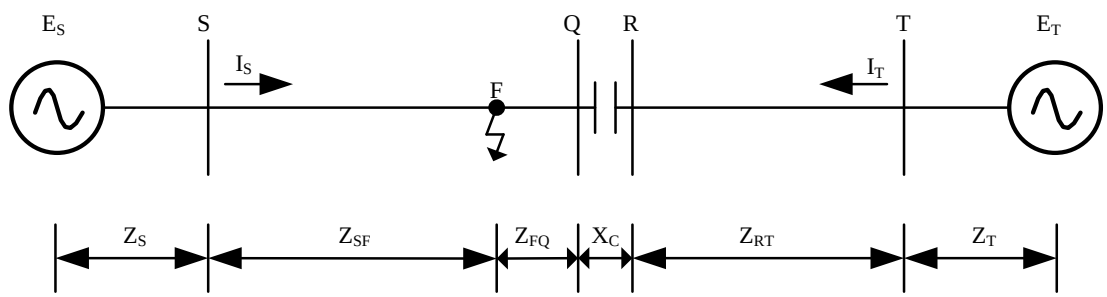

Figure 16. A system with a series capacitor bank

If a fault occurs at the point *F* in the line *SQ*, the voltage at buses *S*, *Q*, *R* and *T* can be expressed as,

$$V_S = I_S Z_{SF} = \frac{E_S}{Z_S + Z_{SF}} Z_{SF} \tag{10}$$

$$I_T = \frac{E_T}{Z_T + Z_{RT} + Z_{FQ} - jX_C} \tag{11}$$

$$V_Q = I_T Z_{FQ} = \frac{E_T}{Z_T + Z_{RT} + Z_{FQ} - jX_C} Z_{FQ} \tag{12}$$

$$V_R = I_T (Z_{FQ} - jX_C) = \frac{E_T}{Z_T + Z_{RT} + Z_{FQ} - jX_C} (Z_{FQ} - jX_C) \tag{13}$$

$$V_T = I_T (Z_{RT} + Z_{FQ} - jX_C) = \frac{E_T}{Z_T + Z_{RT} + Z_{FQ} - jX_C} (Z_{RT} + Z_{FQ} - jX_C) \tag{14}$$

If not considering the resistances, V_R would have 180 degree angle difference with E_T if the following condition is true,

$$X_{FQ} < X_C < X_{FQ} + X_{RT} + X_T \tag{15}$$

The voltage profile during the voltage inversion is shown in Figure 17.

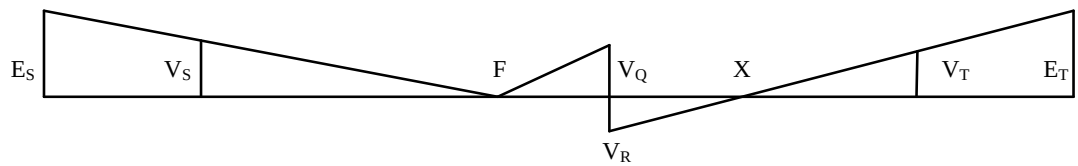

Figure 17. Voltage profile during voltage inversion

The following factors can be concluded for the line *SR* which includes the series capacitor and has an internal fault,

- The occurrence of voltage inversion depends on the fault location, if the fault point is far away from the capacitor where $X_{FQ}>X_C$, there would have no voltage inversion.
- If there is a voltage inversion, the bus side voltage (V_R in Figure 17) has 180 degree angle difference from the source voltage (E_T in Figure 17).
- At the boundary condition where $X_{FQ}=X_C$, $V_R=0$.
- If there is a voltage inversion, the line side voltage (V_Q in Figure 17) has no inversion.

The following factors can be concluded for the line *RT*,

- If there is a voltage inversion on V_R, the voltage at the point *X* is zero. Therefore, the relay at the bus *T* may consider this external fault as an internal fault.
- Similarly, the line side voltage (V_Q) may experience the voltage inversion if there is a fault in the line *RT*, but no inversion for the bus voltage (V_R).

The following figures demonstrate an example of voltage inversion and angle changing transient during a voltage inversion.

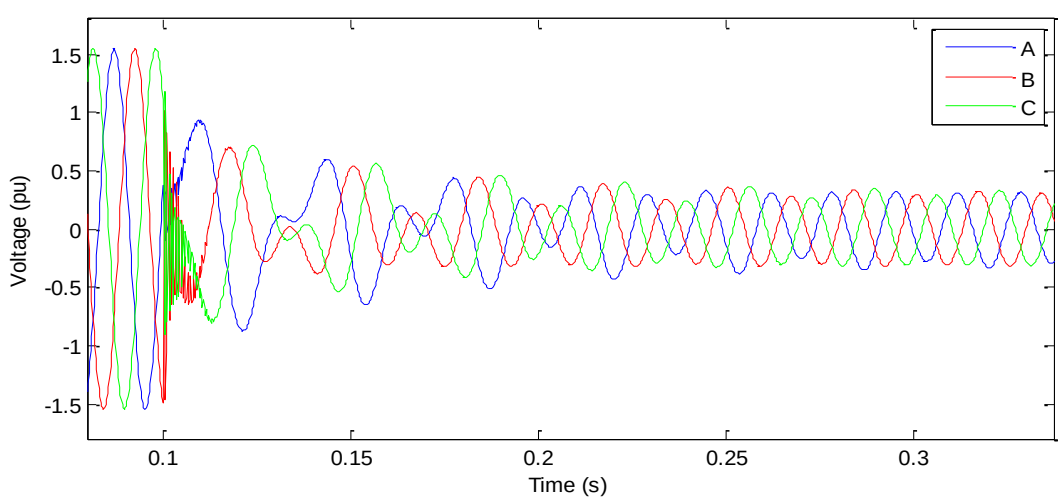

Figure 18. Voltage waveforms during a voltage inversion

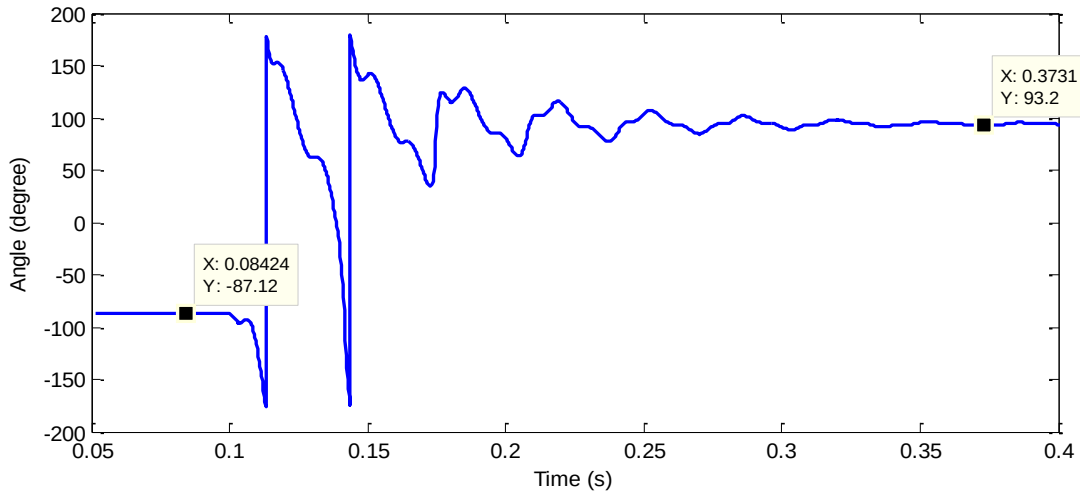

Figure 19. Phase-A voltage angle transient during a voltage inversion

2) ***Current inversion***

It can be observed from Eq. (11) that the current I_T would have the inverse direction if

$$X_C > X_{FQ} + X_{RT} + X_T \tag{16}$$

The voltage profile during this current inversion is shown in Figure 20.

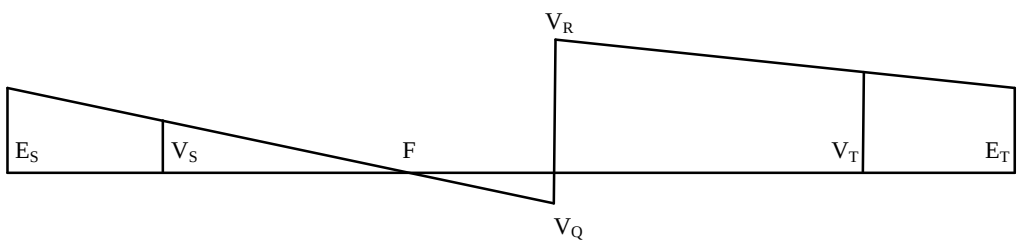

Figure 20. Voltage profile during current inversion

The following factors can be concluded,

- The occurrence of current inversion depends on the fault location and the total backward reactance. If $X_C < X_{RT} + X_T$, there would have no current inversion.
- In the most operating conditions, $X_C < X_{RT} + X_T$.
- If there is current inversion, the line side voltage (V_Q in Figure 20) would have voltage inversion as well.

The figures below demonstrate an example of current inversion and comparison of angle changing with and without current inversion. It is shown as well that the line voltage experiences the voltage inversion during the current inversion, but the bus voltage has no inversion.

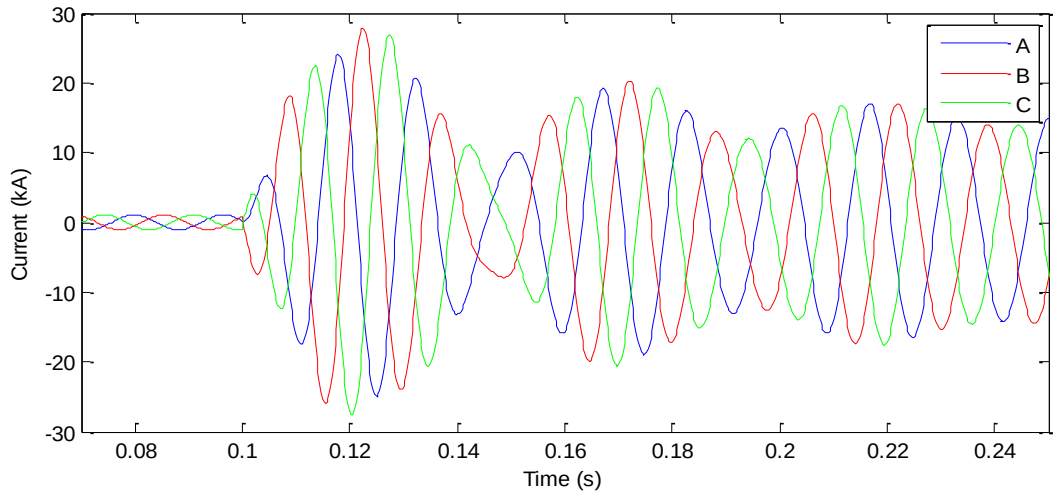

Figure 21. Current waveforms during a current inversion

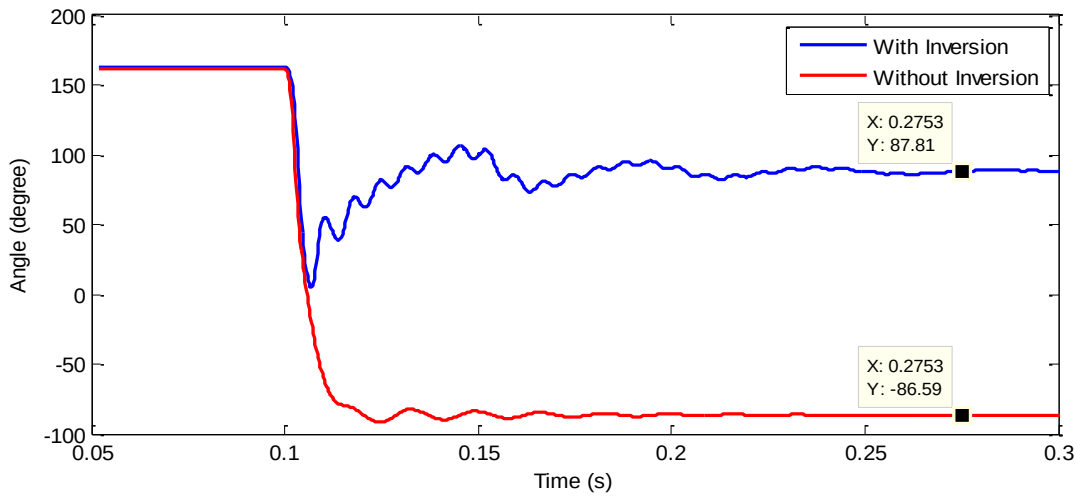

Figure 22. Comparison of current angles with and without current inversion

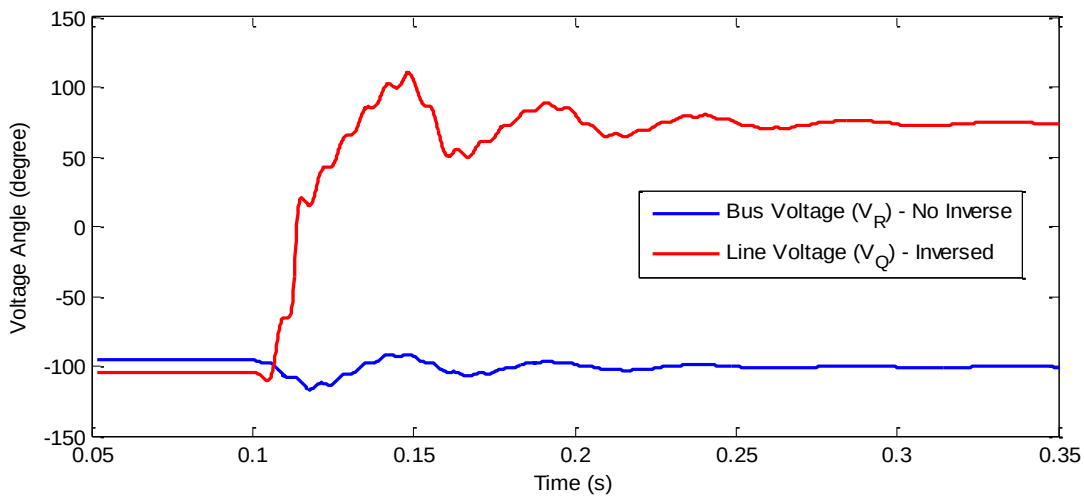

Figure 23. Line voltage inversion during a current inversion

3) ***Sub-harmonic frequency transients***

If neglecting the line shunt capacitance, the system in Figure 16 can be simplified to a simple RLC circuit as shown below,

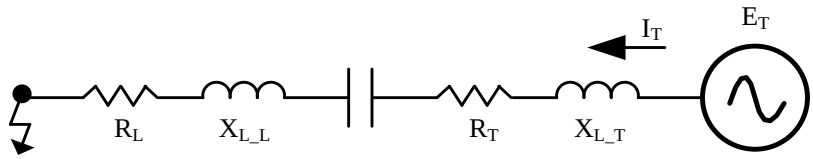

Figure 24. Simplified system

The circuit equation of the simplified system can be expressed as,

$$Ri_T(t) + L\frac{di_T(t)}{dt} + \frac{1}{C}\int i_T(t)dt = E_T \sin(\omega t + \alpha) \tag{17}$$

where, R is the summation of line resistance and source resistance, L is the summation of line inductance and source inductance, C is the capacitance of the series capacitor bank, and α is the fault inception angle.

Solving the above equation, the fault current consists of the steady state part and sub-harmonic frequency transient part, and the simplified form is given as,

$$i_T(t) = I_T \sin(\omega t + \alpha - \varphi) + \left(A\sin\omega_0 t + B\cos\omega_0 t\right)e^{-t/\tau} \tag{18}$$

where, I_T is the magnitude of the steady state fault current,

$$I_T = \frac{E_T}{\sqrt{R^2 + \left(\omega L - 1/\omega C\right)^2}} \tag{19}$$

φ is the angle of the steady state fault current,

$$\varphi = arctg\frac{\omega L - 1/\omega C}{R} \tag{20}$$

ω_0 is the oscillating angular frequency of sub-harmonic frequency transient current,

$$\omega_0 = \omega\sqrt{\frac{X_C}{X_L}} \tag{21}$$

where, $X_L = X_{L_L} + X_{L_T}$.

τ is the decaying time constant of transient current,

$$\tau = \frac{2L}{R} \tag{22}$$

A and B are,

$$A = \frac{E_T}{\omega_0 L}\sin\alpha - I_T\left(\frac{\omega}{\omega_0}\cos(\alpha-\varphi) + \frac{1}{\omega_0\tau}\sin(\alpha-\varphi)\right) \tag{23}$$

$$B = -I_T \sin(\alpha - \varphi) \tag{24}$$

It can be concluded that,

- The frequency of sub-harmonic frequency transient current is normally less than the power frequency because of $X_C < X_L$ in Eq. (21).
- The decaying time constant is two times the time constant of fundamental component, as shown in Eq. (22).
- The magnitude of sub-harmonic frequency transient current depends on source parameters, line parameters, capacitor compensation degree, and fault inception angle.
- The zero fault inception angle would result in the largest transient current, and the 90 degree angle would result in the smallest transient current.

III. Line Differential Application and Solution

The shunt reactors and series capacitor banks introduce impacts on the protections, such as line distance relay, line current differential relay, and directional relay, etc. [5]. This section is only focusing on the application of line differential relay on the line with shunt reactors and series capacitor banks installed.

In the all studies, the traditional dual slope percentage differential scheme is implemented. The differential (operating) signal for an N-terminal line is defined as,

$$I_{DIFF} = |I_1 + I_2 + ...I_N| \tag{25}$$

The restraint signal is given as,

$$I_{RES} = |I_1| + |I_2| + ... + |I_N| \tag{26}$$

The operating conditions are the differential signal exceeds a constant pickup level,

$$I_{DIFF} > PKP \tag{27}$$

and exceeds a percentage of the restraining signal,

$$\begin{aligned} &I_{DIFF} > SLOPE1 * I_{RES}, \text{ when } I_{RES} \le Break\ Point \\ &or, \\ &I_{DIFF} > SLOPE2 * I_{RES}, \text{ otherwise} \end{aligned} \tag{28}$$

A. *System studied*

A 320 km 500 kV transmission line is studied. Two identical shunt reactors are installed at both ends, which can compensate 70% of the line shunt capacitance in total. Additionally, two identical series capacitor banks are installed at the locations of 115 km and 105 km from each end, which can compensate 50% of line series reactance in total.

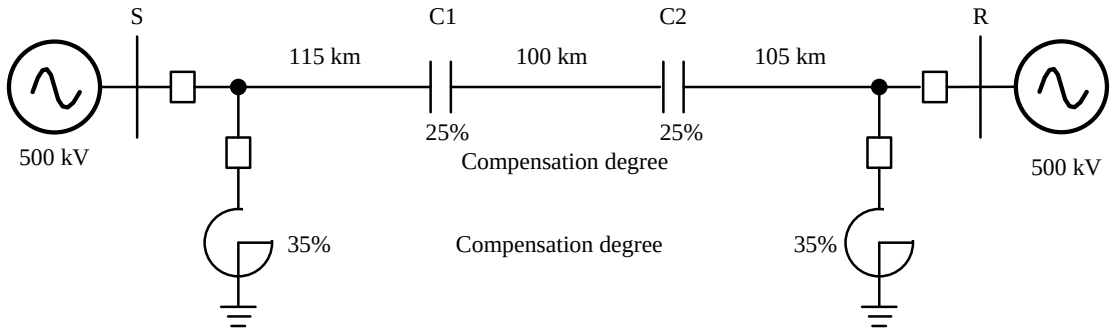

Figure 25. System studied

The parameters in the studied system are given in the following tables.

Table 1: Transmission line parameters

Rated voltage	500 kV
Length	320 km
Positive sequence impedance	116.37 Ω∠ 86.52 º
Positive sequence capacitive reactance	687.8 Ω
Zero sequence impedance	364.1 Ω∠ 71.35 º
Zero sequence capacitive reactance	1100 Ω

Table 2: Shunt reactor parameters

Rated voltage	500 kV
Rated current per phase	147 A
Rated phase reactance	1965.2 Ω
Rated neutral reactance	377 Ω
Rated reactive power	127 MVar
Compensation degree	35%

Table 3: Series capacitor parameters

Rated system voltage	500 kV
Rated current per phase	2200 A
Rated phase reactance	29.04 Ω
Rated capacitor voltage	64 kV
Rated reactive power	422 MVar
Rated MOV energy per phase	52.5 MJ
Compensation degree	25%

B. 87L application with shunt reactors

The reactors may be included or excluded in the 87L line protection zone. This section discusses the effects of these two applications in terms of charging current compensation (CCC), reactor fault, inrush current, and fault transients.

1) Charging current compensation

In the normal operating condition, the differential current of a line is equal to the charging current, if the charging current compensation is not applied. However, since the shunt reactor is designed to compensate the line shunt capacitance, the differential current would decrease to the uncompensated charging current when the shunt reactors are included in the line protection zone. For example, the differential current of the test system is around 418.6 A ($500/\sqrt{3}*1.45$) per phase, and 125.6 A when including the shunt reactors. Therefore, it seems that it is not necessary to compensate the charging current in such situation. However, a control scheme may be designed to automatically switch rectors in and out based on the monitoring of the load current and line voltage. So under such a circumstance that the CCC is not applied when the reactor is switched out, the security of 87L may be jeopardized.

When reactors are excluded in the line protection zone, the differential current in the normal condition is always the charging current no matter the reactors are switched in or not. In order to increase the sensitivity of 87L, the charging current needs to be compensated. The detail of one CCC method can be referred to [6].

It should be noted that the CCC method is not applied in the following studies.

2) Reactor fault

If the reactor is included in the protection zone, a fault in the reactor, especially closed to the line terminal of the reactor, may result in the 87L operation of the line protection, which will trip the line out of service first. Sequentially, the reactor protection relay would isolate itself by tripping its own breaker, and then the line may be restored back to service after the successfully auto-reclose. Even the transmission line is out of service only for a short time caused by a reactor fault, the intermittent interruption would impact the stability of power systems.

When the reactor is not included in the protection zone, the 87L cannot see any increase of differential current in the case of reactor faults and the reactor protection would trip its breaker only.

An example below shows the differential currents in both applications, where a fault occurs at the 5% point closed to the line terminal of the reactor. It should be mentioned that the differential current in the bottom figure is the charging current since the CCC method is not applied.

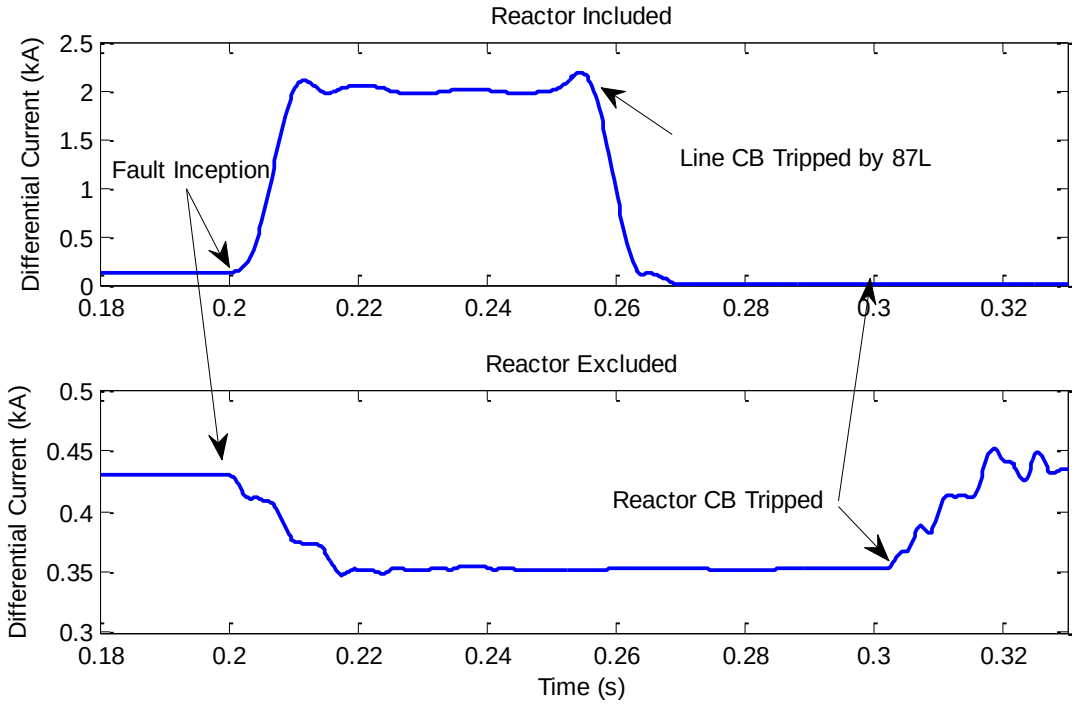

Figure 26. Effects of reactor fault on differential current

3) *Inrush current*

As discussed in Section II-A-1)-b), the 3-pole simultaneous switching-in may result in the inrush current in magnetic-core reactors. This inrush current would not result in the increase of the differential current for both applications as shown in Figure 27, where one group of reactor at the sending terminal is switched in at 0.2 s.

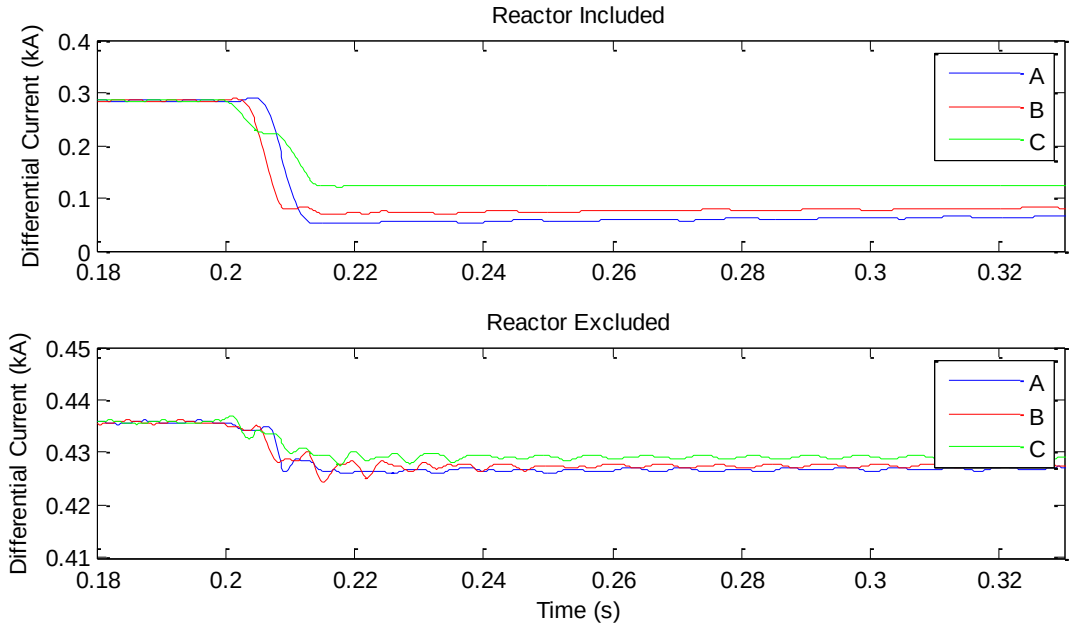

Figure 27. Effects of switching in on differential current

For the application with reactor included, the differential currents decrease because more charging current is compensated by the switched-in reactor. There also has a small increase in the ground differential current because of the unbalance among three-phase differential currents, which is caused by the switching-in operation.

For the application with reactor excluded, the differential currents decrease a little bit because the bus voltage slightly dropped after switching in reactor. There has very small change in the ground differential current, which is nearly zero.

4) Fault transients

The fault current is much larger than reactor current and dominates the differential current. After clearing a fault by a three-pole tripping of the line circuit breaker, the shunt reactor will start resonance with the line shunt capacitance, as mentioned in Section II-A-2)-a/b). This oscillation has no effect on the 87L no matter that the reactor is included in the protection zone or not. An internal fault example is illustrated below. For the application with reactors excluded (the bottom figure in Figure 28), the unbalance in three-phase differential currents after tripping can be eliminated by the charging current compensation.

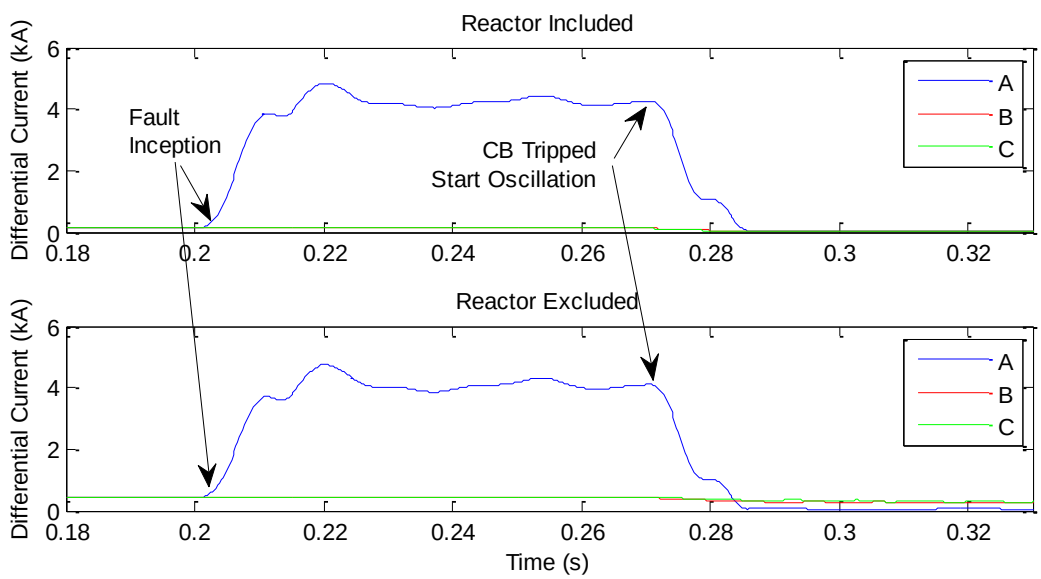

Figure 28. Effects of fault transients on differential current

The external faults may cause CT saturation, which introduces a spurious differential current that may cause the differential protection to misoperate. Typically, a dedicated mechanism is applied to cope with CT saturation and ensure security of protection for external faults. Since this saturation detection scheme is not associated with the application of shunt reactors, the details are not discussed here and can be referred to [6]-[7].

C. 87L application with series capacitors

1) Voltage inversion

If a fault occurs at the point *F* between two capacitor banks in the test system in Fig. 24, the voltage at the bus *S* would experience voltage inversion if the following condition is true,

$$X_{S_C1} + X_{C1_F} < X_{C1} < X_{S_C1} + X_{C1_F} + X_S \tag{29}$$

However, the reactance of the capacitor is designed to be one fourth of X_{S_R}, and $X_{S_C1} \approx X_{S_R}/3$. Therefore, $X_{S_C1}+X_{C1_F}$ is always greater than X_{C1}, it is unlike that there would occur voltage inversion at the bus *S*. The similar conclusion can be made for the bus *R* as well.

If a fault occurs at the point *F* between the bus *S* and the capacitor bank *C1*, the voltage at the bus *S* would not experience voltage inversion and the voltage at the bus *R* would experience voltage inversion if the following condition is true,

$$X_{R_C2} + X_{C2_C1} + X_{C1_F} < X_{C1} + X_{C2} < X_{R_C2} + X_{C2_C1} + X_{C1_F} + X_R \tag{30}$$

Based on the similar reason, there is no voltage inversion at the bus *R*.

To be more generalized, the capacitor banks may be installed at the ends of transmission line or the compensation degree is large in some applications. Then it would be possible that the bus voltage has inversion for an internal fault. Since the use of voltage measurements in 87L is mostly to remove the charging current, the voltage inversion at one end can be equivalently considered as the charging current is not fully compensated, or even not compensated at all. However, the fault current dominates the differential current and the charging current is negligible.

2) ***Current inversion***

If a fault occurs at the point *F* between the two capacitor banks in the test system in Figure 25, the current at the sending terminal would experience current inversion if the following condition is true,

$$X_{C1} > X_{S_C1} + X_{C1_F} + X_S \tag{31}$$

Obviously, this condition is not true for the test system since X_{S_C1} is always greater than X_{C1}.

More generally, in the cases that the current inversion occurs, it may cause the 87LP fail to trip for an internal fault because the inversed current appears to be through current.

Here is an example. Assuming that 1) the same line in the test system is used, 2) one capacitor is installed at the sending terminal and compensation degree is 50%, 3) there is no shunt reactor, 4) the source impedance is ignored (worst inversion case), 5) the fault type is three-phase fault, and 6) the MOV is not conducted during faults. The phase differential-restraint characteristic is shown in the percentage differential plane in Figure 29. It can be observed that the phase 87L may not operate for internal faults located in the 0-30% line section (all blue dots and a portion of red dots) when using the boundary settings (pickup level = 0.5pu, break point = 3pu, restraint slope 1 = 30%, and restraint slope 2 = 60%) illustrated in the figure.

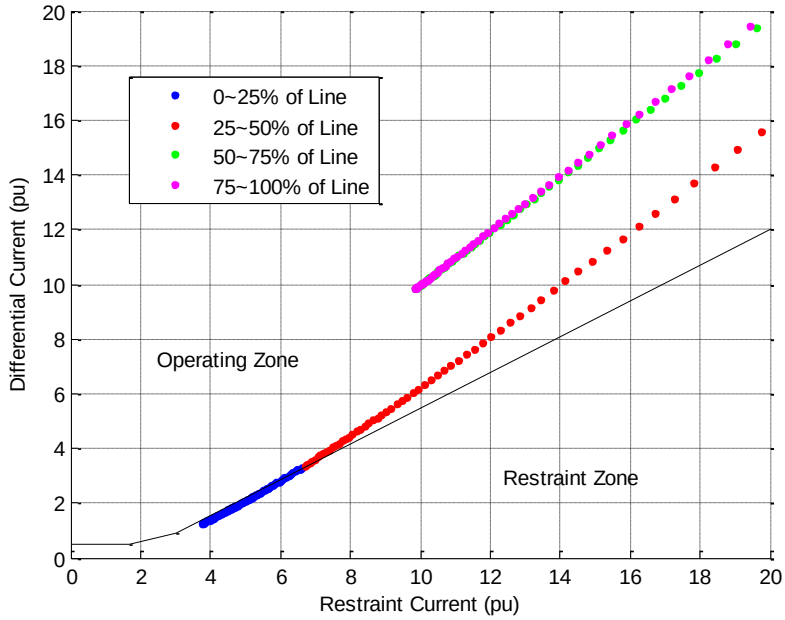

Figure 29. Effects of current inversion on 87LP

If considering the different source impedances, the phase differential-restraint characteristics for faults located in the 0-25% section are illustrated in Figure 30. It can be observed that there has no failure to operate under the same boundary settings. The effect of MOV conducting will be discussed in Section III-C-4).

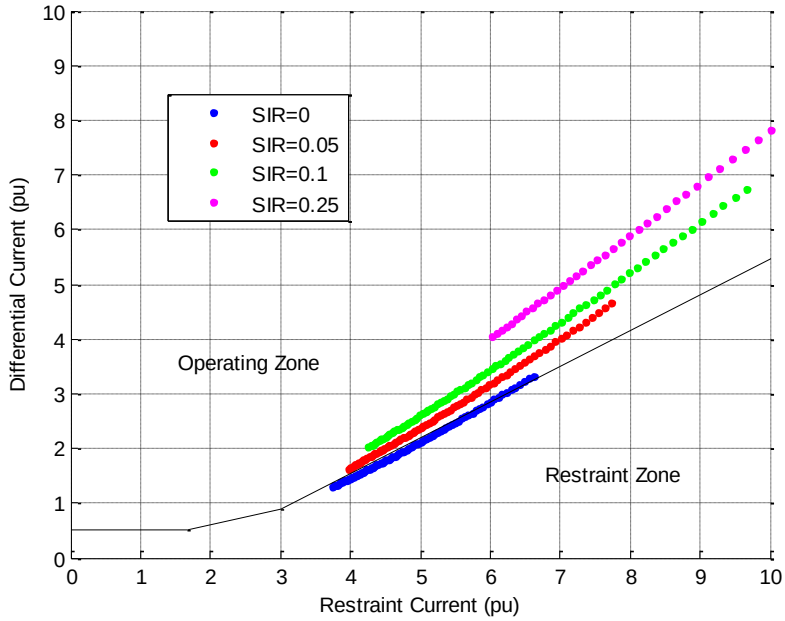

Figure 30. Effects of current inversion on 87LP when considering SIR

Taking SIR=0.1 as an example, the current angles at both ends are illustrated in the following figure. The current angle at the sending terminal has the largest angle inversion when a fault occurs right behind the capacitor bank, and it is reduced to zero at 40 % of the line.

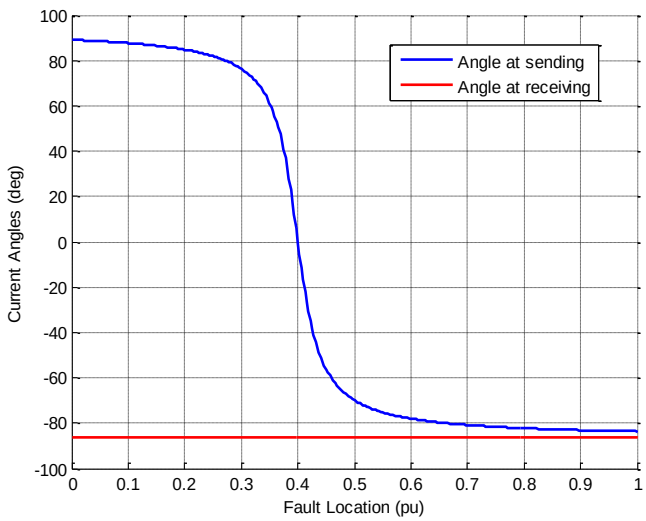

Figure 31. Current angles at both ends when considering different fault locations

Furthermore, with regard to a specified system where the current inversion is possible, it is better to study the system carefully and adjust the boundary settings in the percentage plane to avoid failure to operate during the current inversion.

The element 87LG is usually designed to detect high-resistive (low fault current) ground faults, during which MOV may not be conducted at all. The performance of 87LG is more complicated to be analyzed under such condition. The high fault resistance would add comparatively large component to the resistive part of the fault loop impedance, which may decrease the inversion angle significantly. The inversion angle is defined as the difference of the fault current angle with capacitor and the angle without capacitor installed.

Using the same case mentioned in Section II-B-2), the inversion angles under different fault resistances of an SLG fault are illustrated in Figure 32. It is apparent that the larger fault resistance results in the smaller inversion angle.

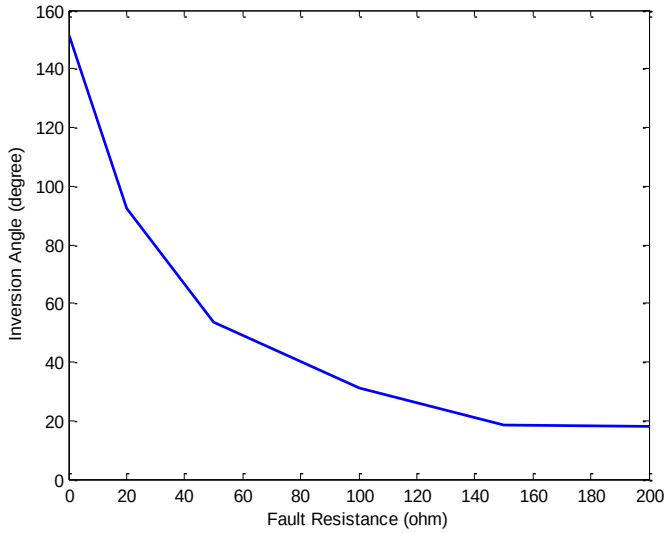

Figure 32. Inversion angles under different fault resistances

Continuing the analysis in Figure 30, a set of SLG faults are studied to examine the effect of the current inversion on 87LG. The SIR is set to 0.1. The ground differential-restraint characteristic is shown in the percentage differential plane in Figure 33, where faults are located at 0-30% of the line section from the sending terminal.

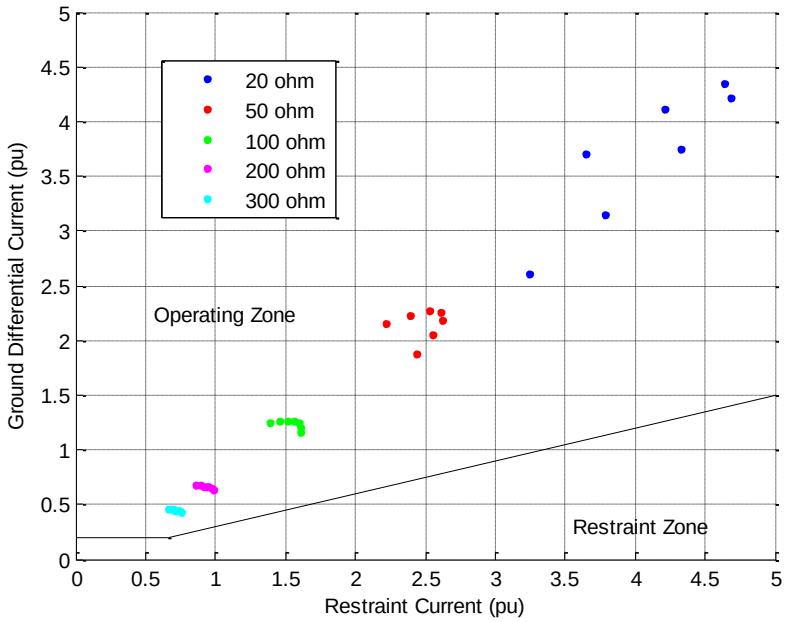

Figure 33. Effects of current inversion on 87LG considering different fault resistances

With respect to the high-resistive faults, even the current inversion may occur, the 87LG may not fail to operate due to the fact that the inversion angle is decreased by the high fault resistance.

3) Sub-harmonic frequency transients

Sub-harmonic frequency transients can result in the slow operation of 87L. The basic reason is that the transients are not eliminated in the DFT calculation; on the contrary, it would introduce more oscillation in the current magnitude. Furthermore, the longer time constant would increase the settling time of the calculated phasor.

A simple simulation is given below for the system with the receiving end open and compares to the same system but with no series capacitor bank. It can be found that the delayed operation time is associated with the fault location. The larger fault distance, the slower operation time. This can be explained that the longer fault distance would introduce the longer time constant as given by Eq. (22). And meanwhile, the lower frequency of transient is resulted as described in Eq. (21).

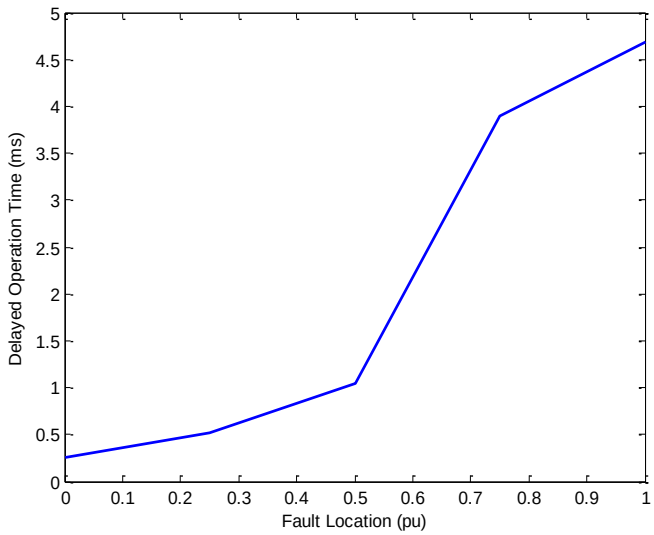

Figure 34. Slow operation caused by sub-harmonic frequency transients

4) ***MOV conducting***

MOV conducting behaves like a variable resistance depending on the voltage across it. Therefore, the capacitor connected MOV in parallel can be approximated to a variable capacitor connected to a variable resistor in series [8].

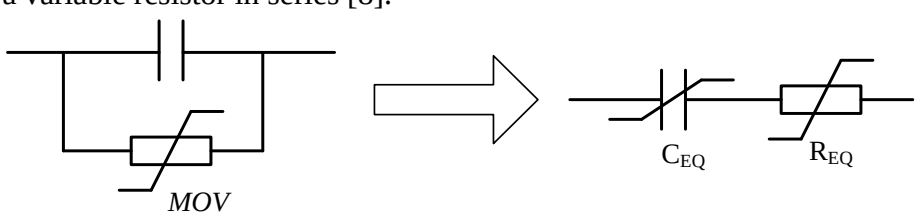

Figure 35. Equivalent circuit of series capacitor when MOV conducts

The equivalent resistance and capacitive reactance are given as below, when $I_{pu}>0.98$,

$$R_{EQ} = X_C(0.0745 + 0.49e^{-0.243I_{pu}} - 35e^{-5I_{pu}} - 0.6e^{-1.4I_{pu}}) \tag{32}$$

$$X_{EQ} = X_C(0.101 - 0.005749I_{pu} + 2.088e^{-0.8566I_{pu}}) \tag{33}$$

$$I_{pu} = \frac{I}{kI_{rate}} \tag{34}$$

where, I_{rate} is the rated capacitor current, I is the RMS value of the fault current, and $k=2\sim3$.

The relation between the fault current and equivalent impedance is shown below.

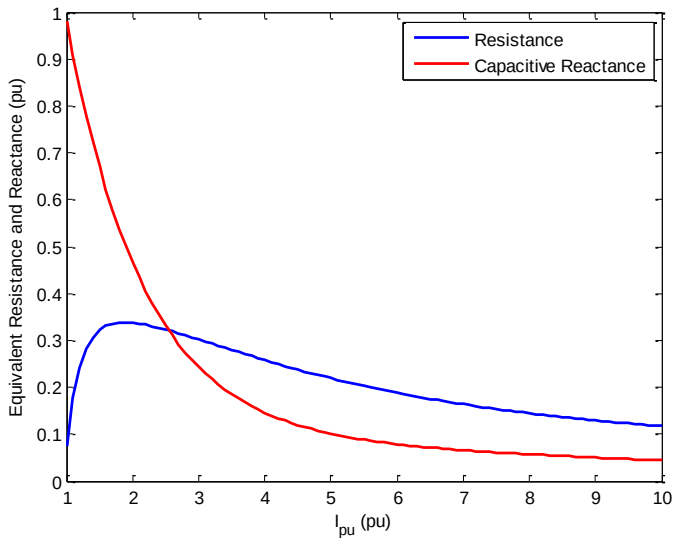

Figure 36. Relation between fault current and equivalent impedance of MOV

Since the equivalent capacitive reactance is becoming smaller when MOV conducts, this will reduce the possibility of voltage inversion or current inversion if existing in a specified system.

Sequence network is analyzed to investigate the effect of MOV conducting on the phase and ground differential relays. Assuming MOV conducts in phase-A, the impedance matrix of three-phase capacitor bank is changed to,

$$Z_C^{ABC} = \begin{bmatrix} (a_1 - ja_2)X_C & 0 & 0 \\ 0 & -jX_C & 0 \\ 0 & 0 & -jX_C \end{bmatrix} \tag{35}$$

where, a_1 and a_2 are the blue and red lines in Figure 36, and both of them are less than 1. The sequence impedance matrix is given as,

$$Z_C^{012} = \frac{X_C}{3}\left(a_1 J_3 - j\left(a_2 J_3 + \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \right) \right) \tag{36}$$

where, J_3 is a 3x3 all-ones matrix. If the capacitor is fully bypassed, $a_1=a_2=0$.

It can be observed that,

- The sequence network is no longer decoupled, which is induced by the asymmetrical MOV conducting.

- Through the mutual coupling, the positive sequence current induces a voltage drop in the zero and negative sequence networks, which is equal to $(a_1+j(1-a_2))* X_C*I_1/3$ and would affect the zero and negative sequence currents.
- The capacitive reactance in the sequence network is decreased to $(a_2+2)/3$ of X_C, which reduces the possibility of voltage inversion or current inversion.
- Since the mutual coupling is inductive, the possibility of voltage inversion or current inversion is further reduced.

Similar to the cases studied in Section III-C-2), a set of SLG faults are simulated, in which the current magnitude is high enough to conduct MOV. The equivalent capacitive reactance is shown in the figure below. The shorter fault distance will result in the larger degree conducting, and in turn the smaller capacitive reactance. It should be mentioned that there is no current inversion in the simulated faults because of the decreasing of the capacitive reactance.

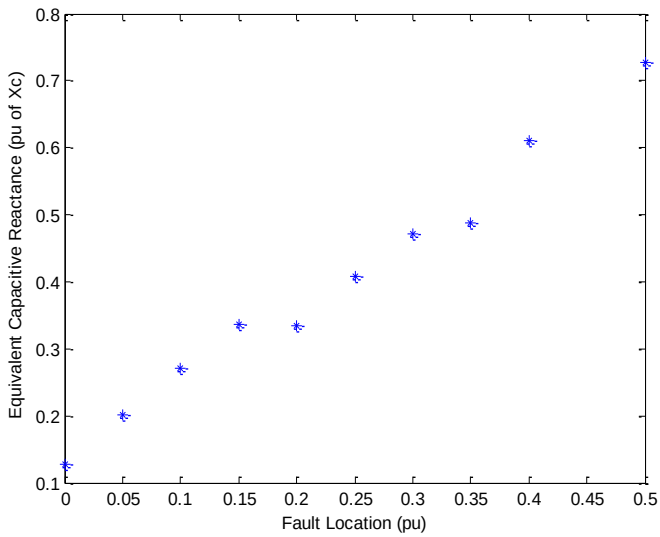

Figure 37. Equivalent capacitive reactance during MOV conducting

The phase and ground differential-restraint characteristic are illustrated in the percentage differential plane below, where SLG faults are located at 0-50% of the line section from the sending terminal.

It can be concluded that,

- MOV conducting would reduce the possibility of current inversion as already discussed in Section III-C-2).
- MOV conducting has no effect on 87LP.
- Basically, it can be considered that MOV conducting has limited effect on 87LG. There are two reasons: 1) 87LG is mostly used to detect low fault current ground faults and MOV may be not conducted under such situation, and 2) the high current faults would decrease the capacitive reactance significantly and the 87LP element should operate for such faults. However, considering a specified system, it is better to have a comprehensive study on the system and adjust differential settings to avoid possible failure to operate.

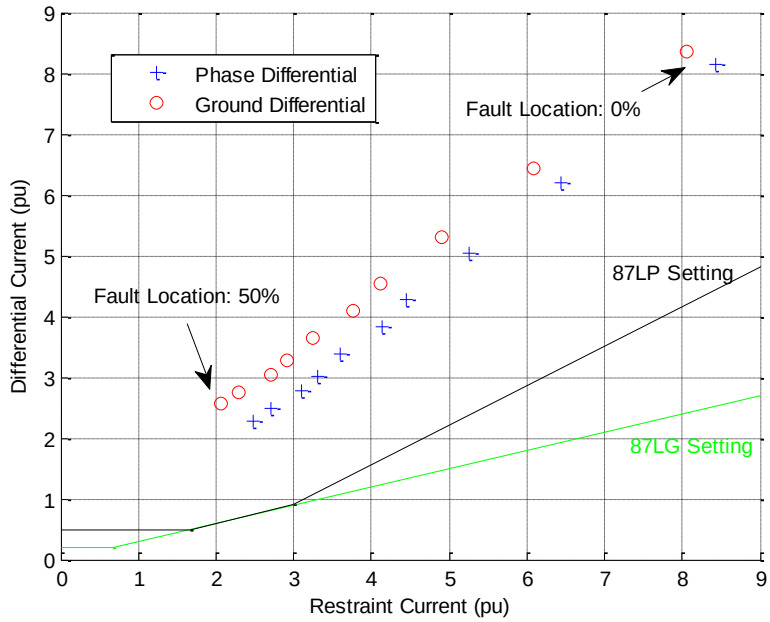

Figure 38. Effects of MOV conducting on 87LP and 87LG

D. Configuration and communication

Based on the analysis in the previous sections, the following recommendations are addressed when implementing the 87L scheme for the transmission line with shunt reactors and series capacitor banks.

- Exclude the shunt reactors in the 87L protection zone;
- Implement the charging current compensation technique;
- Study system carefully and adjust settings to accommodate current inversion if existing and to avoid possible failure to operate;
- Apply both 87LP and 87LG since these elements may respond to the different fault conditions, such that the relay dependability can be increased.

With regard to the test system, two configuration schemes are presented here.

The first scheme is to protect the whole line using two 87L relays over fiber optic communications as shown in Figure 39. The shunt reactors at the both terminals are excluded from the line differential protection zone. If the line length exceeds the typical fiber optic communications range, the multiplexers need to be installed at the series compensation stations.

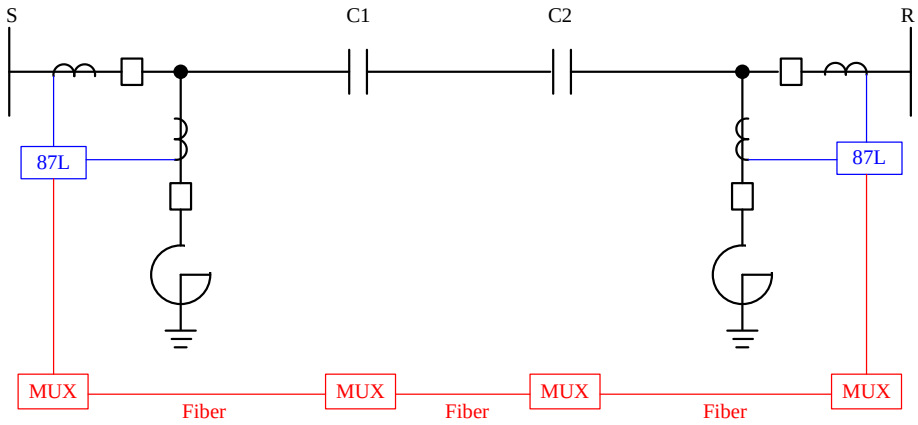

Figure 39. 87L protection scheme for whole line

The disadvantage of the first scheme is that it is hard to determine the fault point, especially located between the two capacitor stations. An alternative scheme is to use three sets of 87L relays to protect each line section as shown in Figure 40. One pair of 87L relays protects one line section communicating via direct fiber optical or multiplexer. The two 87L relays in the capacitor stations have the back-to-back communication. The fault between *S* and *C1* can be detected by 87L1 and 87L2, and a transfer trip signal is sent from 87L2 to 87L6 via 87L3, 87L4 and 87L5, such that the breaker at the terminal *R* can be tripped by 87L6. Similarly, the fault between *R* and *C2* can be detected by 87L5 and 87L6, and a transfer trip signal is sent from 87L5 to 87L1 via 87L4, 87L3 and 87L2, such that the breaker at the terminal *S* can be tripped by 87L1. The fault between the capacitor stations can be detected by 87L3 and 87L4, the trip signals are sent to 87L1 from 87L3 via 87L2, and to 87L6 from 87L4 via 87L5.

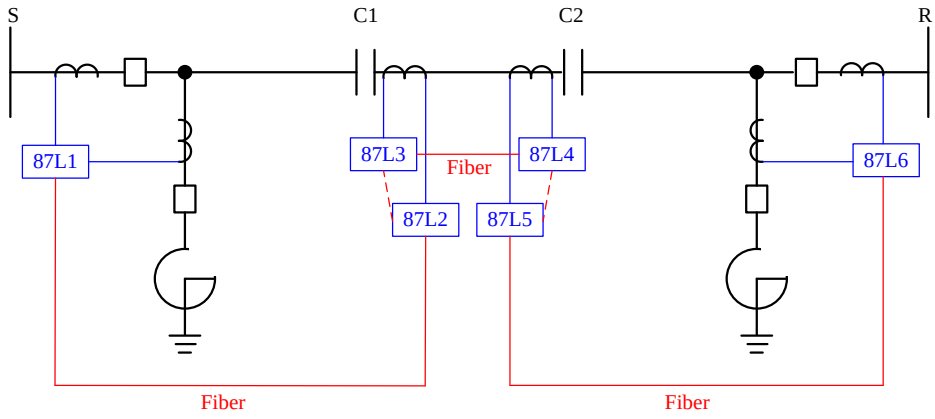

Figure 40. 87L protection scheme per line section

Even the above figures only show one line breaker at each end, more current sources fed into the 87L relay can be handled by the 87L relays, such as in the breaker-and-a-half or ring bus configuration, as shown in Figure 41.

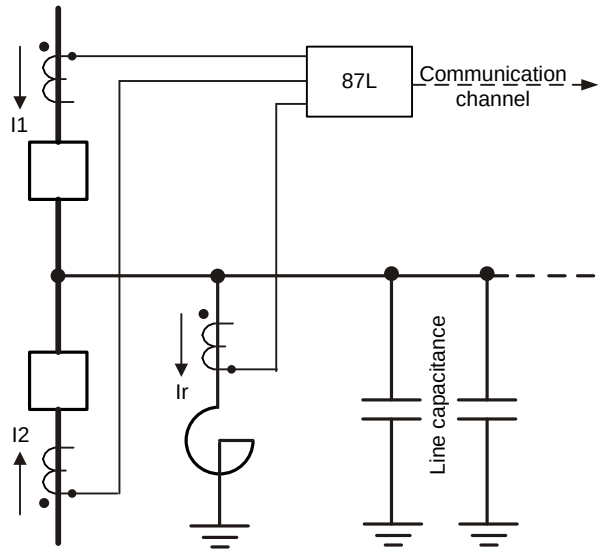

Figure 41. Three current sources application in 87L

Channel failures have to be considered as imminent. Most reliable approach would be having two separate pair of channels such that the failure of one channel would affect not the function of 87L. The two channels can be configured to work in parallel to achieve maximum security and dependability. The channel noise, statistic data of CRC failure and lost packet need to be monitored in real time for each channel, so the primary communication channel can be dynamically switched between two channels in order to improve quality of communication without jeopardizing the performance of 87L.

However, in the case if both channels fail, fallback strategy has to be considered. Modern current differential relays have enough backup elements, like distance, overcurrent, directional etc., to provide essential backup protection for such case.

E. ***Settings***

1) ***Differential settings***

The differential settings in a dual percentage differential plane consist of four settings: pickup level, restraint slope 1, restraint slope 2 and break point.

The pickup level established the sensitivity of the element to high impedance faults, and it is therefore desirable to choose a low level, but this can cause a misoperation for an external fault caused by CT saturation. The selection of this setting is influenced by the decision to use charging current compensation. If charging current compensation is enabled, pickup should be set to a minimum of 150% of the steady-state line charging current, to a lower limit of 10% of CT rating. If charging current compensation is disabled, pickup should be set to a minimum of 250% of the steady-state line charging current to a lower limit of 10% of CT rating. If the CT at one terminal can saturate while the CTs at other terminals do not, this setting should be increased by approximately 20 to 50% (depending on how heavily saturated the one CT is while the other CTs are not saturated) of CT rating to prevent operation on a close-in external fault.

The restraint slope 1 is setting controls the element characteristic when current is below the breakpoint, where CT errors and saturation effects are not expected to be significant. The setting is used to provide sensitivity to high impedance internal faults, or when system configuration limits the fault current to low values. A setting of 10 to 20% is appropriate in most cases, but this should be raised to 30% if the CTs can perform quite differently during faults.

The restraint slope 2 controls the element characteristic when current is above the breakpoint, where CT errors and saturation effects are expected to be significant. The setting is used to provide security against high current external faults. A setting of 30 to 40% is appropriate in most cases, but this should be raised to 70% if the CTs can perform quite differently during faults.

The break point controls the threshold where the relay changes from using the restraint 1 to the restraint 2 characteristics. Two approaches can be considered.

- Program the setting to 150 to 200% of the maximum emergency load current on the line, on the assumption that a maintained current above this level is a fault.
- Program the setting below the current level where CT saturation and spurious transient differential currents can be expected.

The first approach gives comparatively more security and less sensitivity; the second approach provides less security for more sensitivity.

2) ***Charging current compensation (CCC) settings***

Theoretically, the line parameters can be estimated by the electromagnetic simulation software which is normally based on the Carson equation [9]. Practically, the line series impedance can be measured and calculated by injecting a set of specific currents at different frequencies at one end and by shorting circuit at another terminal in some specific ways. However, the positive and zero sequence capacitive reactance used to compensate the charging current may not be available.

Utilizing one of benefits of the line differential relay that the synchronized phasors from both terminals are available, a simple method is proposed to calculate the positive sequence and zero sequence capacitive reactance of the line.

The positive sequence capacitive reactance is calculated by using the positive sequence voltages and differential current under the normal operating condition with no charging current compensation,

$$X_{C1} = imag\left(\frac{V_{s1} + V_{r1}}{2(I_{s1} + I_{r1})}\right) \tag{37}$$

where, V_{s1} and V_{r1} are the positive sequence voltages at the sending terminal and receiving terminal, and $I_{s1} + I_{r1}$ is the positive sequence differential current.

The zero sequence capacitive reactance can be calculated by using the zero sequence voltages and currents during an external fault.

$$X_{C0} = imag\left(\frac{V_{s0}+V_{r0}}{2(I_{s0}+I_{r0})}\right) \tag{38}$$

where, V_{s0} and V_{r0} are the zero sequence voltages at the sending terminal and receiving terminal, and I_{s0} and I_{r0} are zero sequence currents calculated at both terminals.

Taking the line in the test system as an example, the estimation errors of positive and zero sequence capacitive reactance are 1.4% and 2.65% respectively, which is mainly caused by the distributed capacitance in nature and lumped capacitance in calculations.

One alternative estimation method to approximate the zero sequence capacitive reactance is to use the typical transmission line parameters listed in [10] if the positive sequence capacitive reactance is already calculated.

Table 4: Typical ratio of X_{C0}/X_{C1}

Voltage level (kV)	X_{C0}/X_{C1}
69	1.897
115	1.568
230	1.511
345	1.507
500	1.559
765	1.445

Considering the distributed parameters, a more accurate method is proposed and the equations are given below,

$$X_{C1} = imag\left(\cosh^{-1}\left(\frac{V_{s1}I_{s1}-V_{r1}I_{r1}}{V_{r1}I_{s1}-V_{s1}I_{r1}}\right) \Big/ \sqrt{\frac{(V_{s1}+V_{r1})(V_{s1}-V_{r1})}{(I_{s1}+I_{r1})(I_{s1}-I_{r1})}}\right) \tag{39}$$

$$X_{C0} = imag\left(\cosh^{-1}\left(\frac{V_{s0}I_{s0}-V_{r0}I_{r0}}{V_{r0}I_{s0}-V_{s0}I_{r0}}\right) \Big/ \sqrt{\frac{(V_{s0}+V_{r0})(V_{s0}-V_{r0})}{(I_{s0}+I_{r0})(I_{s0}-I_{r0})}}\right) \tag{40}$$

The estimation errors for the line in the test system are 0.0054% and 0.037% for the positive and zero sequence capacitive reactance respectively.

Taking the test system as an example, it should be mentioned that the connected shunt reactors have no effect on Eq. (37)-(40) if they are excluded in the protection zone. The series capacitors have no effect on Eq. (37) and (39) since these two equations are only applied in the normal

condition. Also the series capacitors would not affect Eq. (38) and (40) if the three-phase capacitor banks have the same equivalent impedance during the external fault.

IV. CONCLUSIONS

The principles and applications of series capacitor banks and shunt reactors are introduced. Then the impacts of these apparatus on power systems are examined, and the mathematic expressions and simulation examples are presented to give the accurate description of these effects.

Particularly, the impacts on the line differential relays are studied in detail. Based on the analysis and simulation, the recommendations in the following aspects are discussed, which can be implemented in real applications:

- Configurations of the 87L scheme;
- Arrangement of communication channels;
- 87L settings in the percentage differential plane;
- Charging current compensation setting;
- Simple methods to calculate positive and zero sequence capacitive reactance.

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VI. BIOGRAPHIES

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